Design for Testability Guidelines

1.0 Purpose

The purpose of this document is to describe the recommended testability guidelines to be used when designing Printed Circuit Boards (PCB). These guidelines and rules will help ensure that a reliable in-circuit test fixture can be produced.

2.0 Test Probe Node Access

The design should provide 100% test probe access for each net node. A minimum of 1 test target per net and multiple accesses for power nodes is preferred.

2.1 **Signal Node Access** - there must be a minimum of 1 test probe location per net.

2.2 **Node access from one side of board preferred** - All test targets should be accessible from one side of the board. Test fixtures can be fabricated to allow topside test node probing, but this increases fixture cost.

2.3 **Power and Ground Node Access** - the PC board layout must include adequate probing of power and ground nodes. Good power and ground connections are critical to the signal quality of powered tests.

2.4 **Minimum ground Requirement** - There must be a minimum of one ground test target per PC board tester power supply and one ground sense target (2 total). Example: if a PCB requires 3 power supply voltages, there must be a minimum of 4 ground test targets (3 voltages, 1 sense).

In addition to the minimum ground test target requirement, the amount of load current must be considered. The return current through ground is the sum of all of the individual power supply currents. The maximum current load per test target should not exceed 500mA. Example: If the sum currents of the power supplies are 5 amps, then 10 ground targets are required. The ground test targets should physically be evenly distributed if possible.

To ensure good signal integrity, especially during digital testing, multiple ground nodes should be available. A good rule of thumb is to provide a minimum of 10 ground connections plus one additional connection per 20 nodes. Example: for a 1000 node PCB assembly, the number of ground connections should be: 10 + (1000/20) = 60 ground connections.

2.5 **Minimum power supply requirement** - There should be 3 test targets per power supply: 2 for power and 1 for power sense.

Power Supply current considerations - There should be one test target per 500 mA of power supply current load. These test targets should be evenly distributed on the PCB if possible. As a rule of Thumb: provide at least one power and ground test target for every 20 electrical nodes.

2.6 **Digital Grounds** - to help maintain good signal quality for high-speed digital signals, test targets should be evenly distributed on the PCB with a digital ground test target for every 2.0" square area.

2.7 **Unused Component Pins** - providing node access to unused IC leads is preferable but not required. Providing test access to unused pins reduces test development time and increases the test fault coverage as well as reducing manufacturing costs.

2.8 **Etched edge connectors** - should have a plated through hole for all component side connections as close to the edge connector as possible. The edge connector fingers will not normally be used for test probing.

2.9 **Node Access Restrictions** - in some cases adding node access would compromise the functionality of the design. In these cases other testing approaches will be incorporated such as: cluster testing a group of components, boundary scan, or functional testing. When these cases arise the designer should discuss testing methods with the Test Engineer as some design changes may be required to provide adequate test coverage.

3.0 Test Targets

A test target is any surface that can be used by a Test Probe to create an electrical connection between the test fixture and the PC Board under test. The test surface is critical for creating an optimal in-circuit test solution. The Test points need to be identified properly in the PCB CAD database so that the ICT Test Development process produces the optimal result.

3.1 **Test Pad** – is a solid surface without a through-hole. This surface will be an electrical conductor where the test probe will strike the solid surface.

3.2 **Test Via** – is a plated through-hole with and exposed annular ring around it. It is recommended that the Test Via be solder filled. If not solder filled, a test probe must be selected that is capable of making connection with the annular ring of the open via. Large open Vias should be avoided. If the Via drill hole is too large the test probe may pass directly through the open hole thus making no connection.

3.3 **Through-Hole Pin** – is a component device lead. This lead should have a known and consistent length. Probing excessively long lead lengths should be avoided. Test probes should not be placed on through-hole device pins on components that are not placed in all board versions.

3.4 **Test Target Size** – to provide a reliable test probe contact to the PCB surface. A test target size of greater than .035 mils is preferred.

>.035” – Provides optimal probe target size
>.028” – Provides an acceptable probe target size
<.020” - use in extreme cases only

Note: Test pad diameters of less than .025 mils should be minimized

3.5 **Test Target Surface** - the surface to be probed must be solder coated or something conductively equivalent. Test vias should be filled with solder.

3.6 **Solder masks** - Solder masks, silk screens, or stick on labels must not cover Test targets.

3.7 **SMT Component Pins** – SMT leads should not be probed.

3.8 **Probing Connectors** – when probing connectors, it is preferred to probe the solder side of the connector. However, special cupped style probes may probe Male connectors at the pins.

4.0 Test Target Spacing and Clearance

The test target center to center spacing is determined by the physical size of the ICT test probes. The adjacent test points and components also determine the Test probes.

4.1 **Test Probe Sizes** - the test probes available for an ICT test fixture are:

100 mil – Preferred
75 mil – Acceptable
50 mil – minimize use
39 mil – minimize use

4.2 **Test Probe Center to Center Spacing Table**

Probe	To Probe	Minimum Clearance (1/10 mils)
100 Mil probe	100 Mil probe	850
75 Mil probe	100 Mil probe	800
50 Mil probe	100 Mil probe	720
75 Mil probe	75 Mil probe	700
39 Mil probe	100 Mil probe	690
50 Mil probe	75 Mil probe	660
39 Mil probe	75 Mil probe	610
50 Mil probe	50 Mil probe	490
39 Mil probe	50 Mil probe	470
39 Mil probe	39 Mil probe	390
100 Mil probe	375 Mil tooling pin	2850
75 Mil probe	375 Mil tooling pin	2780
50 Mil probe	375 Mil tooling pin	2700
39 Mil probe	375 Mil tooling pin	2700
100 Mil probe	200 Mil tooling pin	1525
75 Mil probe	200 Mil tooling pin	1475
50 Mil probe	200 Mil tooling pin	1275
39 Mil probe	200 Mil tooling pin	1275

4.3 **Test Target Component Clearance** - there must be a minimum .018" annular ring around the edge of a test target that is free of components, exposed metal, other test targets, or obstructions. This clearance minimizes the risk of a test probe shorting to an adjacent component.

4.4 **PC Board Edge Spacing** – Test Targets should be placed .125” away from the edge of the PCB board or from the Panel breakaways.

4.5 **Components on Probe Side of Board** - components on the probing side of the PCB should not exceed **.250"** in height. Components exceeding this height will require special fixture considerations such as cut outs in the fixture plate. If a component height of greater than .250" exists there must be a free area of **.200"** around the component (example: no test pads closer than .200").

4.6 **Test Target Distribution** - test targets should be as evenly distributed across the PCB as possible. The vacuum test fixture must overcome the counter force of the test probes. By evenly distributing the test probes, the PCB under test will remain as flat as possible during the vacuum process.

5.0 Tooling Hole Requirements

All PCB's must have tooling holes to provide orientation of the PCB to the test fixture. These holes should be placed near the opposing corners of the PCB and should not be plated. The edge of tooling holes should be no closer than 0.125 inches to the edge of the P.C. board on P.C. boards greater than 64 square inches and no closer than 0.100 inches on P.C. boards smaller than 64 square inches (where possible). Also, tooling holes should be placed asymmetrically to help prevent improper placement of board on the test fixture. A third tooling hole could also be added to prevent improper placement.

5.1 **Tooling Holes to Test Targets Tolerance:** +/- .002"

5.2 **Number of Tooling Holes**: minimum of 2 holes (preferably on diagonal corners). A third hole that is non-symmetrical may be used to ensure proper orientation of the PCB assembly on the ICT test fixture.

5.3 **Tooling Hole Size**: 0.125” (0.156” for PC board over 96 sq. inches)

5.4 **Tooling Hole Tolerance**: +0.002/-.000” diameter

5.5 **Keep out area around tooling holes:** Components and Test probing locations must maintain clearance from the tooling hole clearance.

0.375” Variable Diameter Tooling Clearance (Preferred)
0.200” Standard Tooling Clearance (Acceptable)

5.6 **Panelized PCBs:** Tooling holes must be provided for the PCB Panel and each of the individual boards.

6.0 PCB Board Assembly Physical Dimensions

The physical size of a PCB should be restricted to the capability of equipment used to build and test the PCB. The requirements for the purpose of testing are:

Standard Fixture with Vacuum Box or Over-Clamp: 11.5" x 14.7"
Standard Fixture with molded gasket: 15.8” x 14.1”
Oversize Fixture with Vacuum Box or Over-Clamp: 26.0" x 14.7"
Oversize Fixture with molded gasket: 15.8” x 28.3”

Note: Special Fixture design will be required for large PC board assemblies

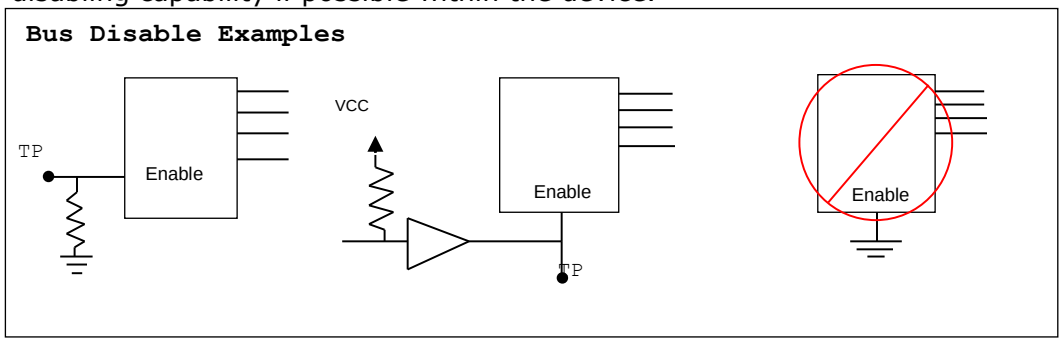
7.0 Electronic Testing Considerations

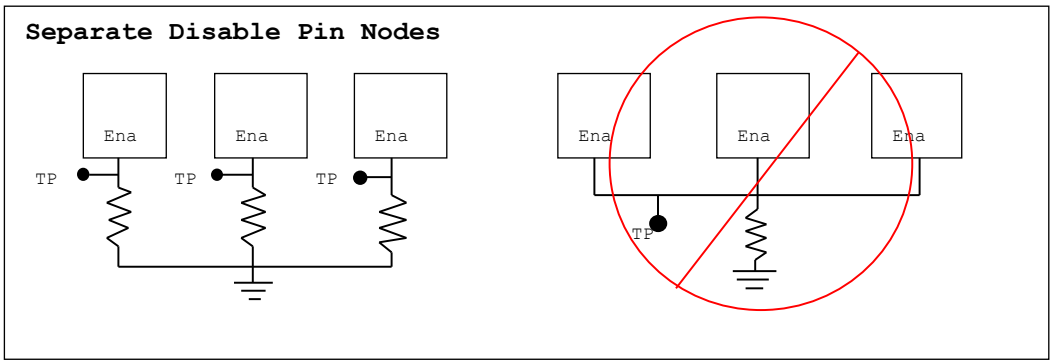
An in-circuit testing strategy is the most common approach incorporated for testing PCBs; as such, implementing common ICT design guidelines will make the PCB easier to manufacture and test.

7.1 **Tri-State Devices –** Device disable pins should never be tied directly to power or ground. Instead, disable pins should be connected via a small value resistor to power or ground. A test probe then needs to be connected to the disable pin node.

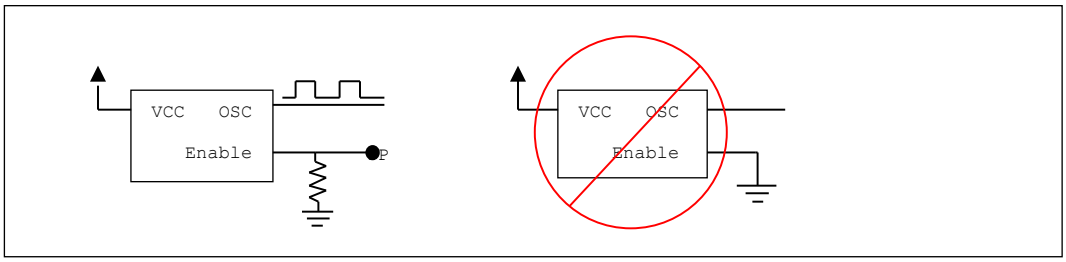
7.2 **Disable bussed devices** - A bus-able device must always have the capability of being disabled by the board tester in order to test other devices sharing the same bus. Disable pins of multiple devices should not be tied together. Each of these devices should have a separate disable node.

7.3 **Disable upstream devices** - Any device that drives other circuitry on a board that has the capability of being disabled should be designed such that the tester can disable it. This will relieve the device from the stress of being back driven by the tester. Programmable devices or PLD’s should incorporate a disabling capability if possible within the device.





7.4 **Disable free running clocks** - Free running devices such as oscillators, crystals, or clock circuitry can prevent upstream devices from being tested adequately. These circuits must provide a disabling method. The preferable method is to electrically disable the circuit where possible.



7.5 **Use semiconductor device packages that provide disable pins** - Many electronic devices provide packages that include a test pin or a group of test pins (example: Intel 80386, Motorola 68040). When asserted these devices can be tri-stated or placed in a known condition. These features should be included in the design when possible.

7.6 **Custom or Programmable Devices** - ATE tests for programmable devices are developed one of two ways: the first way is totally automatic using the appropriate device files, the second way is to manually code the test from the equations supplied. Tests for most of the commonly used PAL's can be generated from the fuse map files. Other software packages exist which can provide an automatically created device test library. In either case the **appropriate files must be supplied to generate the test code.**

7.7 **Use of Boundary Scan Parts** – many programmable devices such as FPGA's, PLD's and Micro's are now available with boundary scan included. Often the BSDL code, which can be converted to test code automatically, is available from the manufacturer. Use of boundary scan will greatly reduce test development time as well as solve node access problems. Boundary scan does require some design effort but should be considered.

7.8 **Devices with External Access Pins -** Some Micro's have external access pins that determine whether code will be executed internal to the device or externally. This device pin **should not** be tied directly to a power or ground net. Most ATE device libraries for Micro's are coded for external access.

7.9 **Digital Feedback Loops** - during an in-circuit test digital devices are tested individually, where the device under test is isolated from the surrounding devices by a method known as back driving. This form of testing usually isolates a failure down to the component level. It is difficult to isolate a device if an output of the device is directly or indirectly fed back into the input of the same device. For example: the clock output of a micro being fed into a ready input via a flip-flop. In cases like these pre-conditioning or disabling the device that feeds the input would remove the isolation problem.

7.10 **Analog Feedback Loops** - feedback conditions often occur in analog device circuits. Breaking up this circuitry may be helpful in isolating faults;

however, this is not usually an issue since analog circuits are tested in a more functional approach.

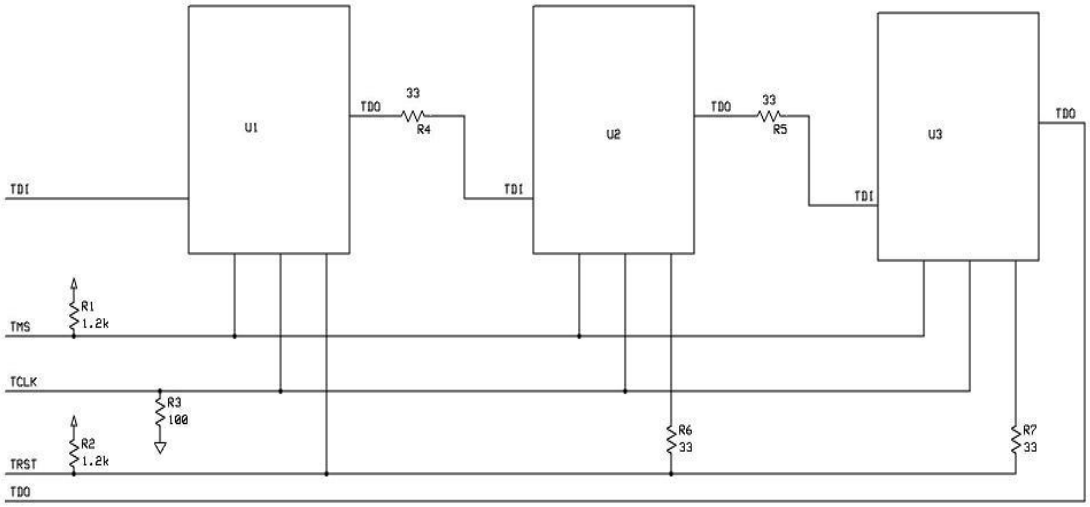
7.11 **Device Control Pins** – do not connect IC control pins directly to power or ground. Instead used a common pull-up or pull-down resistor.

7.12 **Batteries** – should be removed or isolated during ICT test. Battery voltages interfere with un-powered component testing. Also, shorts can not be detected in battery circuits.

Note: Remember, all of the above suggestions are meant to improve testability by reducing development time, troubleshooting time, and manufacturing costs. They however are not meant to hinder the functionality of the design.

8.0 Testing Boundary Scan Components

For the purposes of In-circuit Testing (ICT) all JTAG port pins of a Boundary Scan device must be test node accessible. All JTAG ports contain a minimum of four test pins: TCLK, TMS, TDI, and TDO. Some Boundary Scan devices contain an additional TRST pin. If multiple Boundary Scan devices are used in a circuit design, then each device should be connected in a boundary scan chain as is shown in the diagram below. The resistors shown below are not required but may be beneficial during ICT testing.



Recommendation 1: Make as many device pins test accessible as possible.

Recommendation 2: Add a series resistor between the TDO and TDI pins in each element of a boundary scan chain. A boundary scan test has a relatively long execution time. A series resistor will reduce the back drive current into the upstream drive. Note: you still need to make all JTAG nodes accessible.

Recommendation 3: If the **TRST** node provides a method of disabling the boundary scan device, then each device should be able to be disabled individually. This way, each boundary scan part can be tested individually while the other boundary scan parts are disabled. Remember, TRST is not available on all boundary scan IC's.

9. ICT Documentation Recommendations

To develop an ICT test, the documentation package must include a readable Schematic (usually in PDF form), a BOM in spreadsheet or text ASCII format, and an ASCII CAD file.

9.1 **The BOM** – must include the reference designator name, manufacturer part number, values and tolerances. A text ASCII or Excel Spreadsheet is preferred

9.2 **CAD Design Files –** the Cad documentation may be a single database file or multiple output test files depending on the CAD system used. CAD files must contain the following information:

- Component reference designator and pin number
- Component side location (primary or secondary)
- Node name of each component pin
- X-Y locations of all component pins
- X-Y locations of all via's and associated node name or node number
- X-Y location of all test points and the associated node name or node number

Common CAD System and associated files:

PADS	.ASC (Version 5.0 or older)
PCAD	.PDF
Accel	.PCB
Cadence / Allegro Extract	.BRD, .PAD, .SYM and .RTE
Mentor Neutral	.NEU
Orcad	.MIN
Gencad	.CAD
ODB++	.tqz, .gz, .zip
IPC356	.txt
Protel PCB Ascii	.PCB
Fabmaster Device ASCII	.ASC
Zuken PSW (CR3000/CR5000)Layout	.BSF

10.0 Optional Testing Techniques

10.1 **Vectorless Test** (Test Jet and VTEP) – for testing the placement and solder connections of complex digital devices and connectors.

10.2 **Polarity Check** – polarized capacitors are check for proper polarity

10.3 **Switch Probes** – Checks presence of connectors etc.

10.4 **LED Color Testing** – Tests for LED Color and Intensity

11.0 Panel Testing

A panel test may be any number of combinations of an individual board. The typical configuration is a multiple number of the same board type. A panel test may also be several types of boards. For a **Multi-Same board panel** configuration you should provide a panel drawing and Gerber panel files to determine X-Y offsets and position for each board. The number of boards to test on an ICT fixture will be restricted to the node capacity of the test system, the power supply capacity, and the fixture area size. In some cases fixture electronics will be needed to distribute and isolate power to each individual board under test.

12.0 Artwork Revision Guidelines

It is possible to update an ICT Test fixture when artwork revisions are made to a PC board. The following guidelines will help ensure the that a fixture upgrade will be possible

- Do not move Tooling holes
- Do not move test pad locations unless absolutely necessary
- Do not rename reference designators
- Do not rename node name
- Rename the nets that have changed
- Attempt to place new test pads at least 0.100” from existing test pads.